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NEMS switches monolithically fabricated on CMOS MIM capacitors

J.L. Muñoz-Gamarra, A. Uranga, N.Barniol

Electronic Engineering Department, Universidad Autonoma de Barcelona, 08193 Bellaterra, Spain

Abstract

This work demonstrates the monolithically integration of NEMS structures in a commercial CMOS technology. Low voltage operating switches (5 V) have been obtained thanks to the definition of a small structure (1.5 µm length, 500 nm width) and a small gap (27 nm), using the MIM module of an analog CMOS technology (AMS 0. 35 µm). In this way NEMS can be fabricated taking advantage of the robust and reproducible CMOS fabrication process.

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Keywords: CMOS-NEMS, Electromechanical switches, TiN

1. Introduction

The use of CMOS-MEMS has been expanded in Microelectromechanical systems field thanks to the robustness and reproducibility of its fabrication process, easy integration with additional circuitry and mass production capability. They have been successfully implanted in such diverse field as mass sensing [1], RF modules [2] or fluidics applications [3]. Recently, some efforts have been carried out in order to expand its use to the field of mechanical switches [4].

Microelectromechanical switches have emerged as a solution to the passive power consumption increase as the CMOS technology nodes are reduced, due to leakage gate and sub-threshold currents, and that is slowing down the scaling pace of CMOS technologies according to Moore's law [5]. N/MEMS switches are composed by a mobile structure that is deflected until it reaches physical contact with an electrode, forming a path for the current to flow.

Corresponding author. Tel.: + 00 34 93 581 13 61; fax. +00 34 93 581 26 00
E-mail address: Nuria.Barniol@uab.es

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In the OFF state (no contact between the beam and electrode), the current is limited to vacuum tunnelling and Brownian motion displacement currents that appear in the physical gap that separates the mobile structure and the electrode. These currents are very small solving the problem of passive power consumption that traditional CMOS transistors present.

The ON state is achieved when the voltage difference between the mobile structure and driver produces an electrostatic force bigger than the elastic restoring force, collapsing the mobile structure with the electrode. This snap-in or pull-in voltage, $V_{SNAP\text{-}IN}$, depends on the Young modulus, E, the thickness, t, and length, l, of the structure and the gap between movable structure and driver, s, according to equation (1), (for an out of plane configuration) .

$$V_{SNAP-IN} \propto \sqrt{E\frac{s^3t^3}{l^4}} \qquad (1)$$

So it is clear that in order to reduce the operating voltages small thickness and gaps are required. Moreover, the operation at low voltages reduces the damage of the structure by field emission or joule effect due to high current when the beam is brought into contact with the electrode [6].

Trying to develop high performance switches at low snap-in voltages, bottom-up and top-down switches fabrication approaches have been used, as it is summarized on table 1. In this table the main characteristics of the state of the art switches are showed. Note that just the devices that present small dimensions, and thus large integrability, are shown although some of its features are improved by other top-down devices with big coupling area [7-9].

Table 1. Nano-electromechanical switches state of the art.

Approach	Material	Length(um)	Gap(nm)	Vpull-in	Ion/Ioff	Ron (Ω)	mV/decade	CMOS
BOTTOM-UP	Carbon Nanotubes [10]	2	30	4.15V	10^5	---------	-----------	NO
	Carbon Nanotubes [11]	0.130	20	3.5V	10^4	--------	--------	NO
	Silicon Nanowires [12]	1-25	500	19V	10^2	---------	----------	NO
TOP-DOWN	Silicon Carbide [13]	6-20	27nm-90nm	1V-8V	10^3	from k to M	--------	NO
	TiW/W [14]	1.5	4nm	0.4V	10^6	X	10	Hyb.
	Pt [15]	3.5	100	4.3V	10^4	10M	0.8	NEMS on CMOS
	TiN [16]	0.3	15	14V	10^5	X	3	CMOS compatible

1. Fabrication process

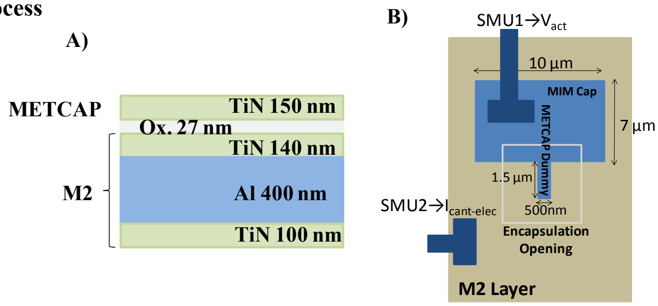

Figure. 1. (A) Schematic view of a MIM module cross-section; (B) METCAP dummy element for implement NEMS cantilever. It can be observed how to release just the cantilever an opening in the encapsulation is defined above it (white square), preventing the releasing of the anchor.

In order to reduce the dimensions of the micro-electromechanical switches previously developed in CMOS technologies [4], a capacitive metal-insulator-metal (MIM) module has been used in order to define out of plane two terminals (2-T) switches. This module is composed by two conductive layers. The top layer, METCAP, is based on TiN and it has a thickness of 150 nm separated by a 27 nm dielectric layer (figure 1 A). Out-of-plane mechanical structures can be defined using this top layer. The driver electrode will be the Metal 2 layer of the CMOS technology, with a TiN layer as the metal contact. The technological design rules fix a minimum capacitance area of 4 µm x 4 µm. In order to overcome this problem, a dummy structure is defined attached to a capacitance, acting like the mobile structure (Figure 1 B)). In this way, small dimensions (with a minimum width of 500 nm) are obtained. The releasing of the NEMS switch is based on a buffered HF wet etching without any mask protection as it has been previously reported [1-4]. 2-T switches based on these cantilever structures with different lengths were fabricated (2.5 µm, 2µm and 1.5 µm).

Figure 2 A) shows the SEM images of a 1.5 µm long cantilever NEMS switch. Figure 2 B) shows a tilted SEM image of a released and stuck device corresponding to a length of 2 um (note how the gap is appreciated below the anchor area and how it disappears below the cantilever area).

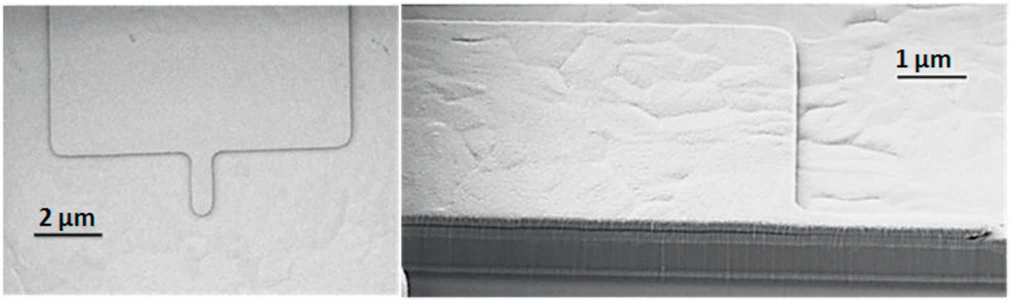

Figure. 2. (A) SEM image of a 1.5 µm length B) Cross section SEM image of a released and stuck 2 µm cantilever after a FIB cut. An air gap, corresponding to the 27nm gap, can be appreciated between the anchor and the driver.

2. Electrical characterization

The 2-T switches were characterized with a semiconductor Devices Analyzer (Agilent B1500A) applying a voltage difference between the cantilever (0 V) and the electrode (where a voltage sweep was applied) (Figure 1 B)). In addition a 500 MΩ resistance was added in series with the cantilever in order to prevent the damage of the structure by high currents when the contact is established. The current in both terminals were acquired. In figure 3 A) the electrical response for different length designs is shown. It can be appreciated how as longer is the beam, smaller snap-in voltages are obtained, 19 V (l=1.5 µm), 16.7V (l=2.0 µm) and 11.6V (l=2.5 µm) . Additionally, it can be observed, how the snap-out voltage is bigger as shorter is the structure length. The elastic constant of the structure is bigger as the length is reduced, which implies that the forces at contact (Van der Waals forces and electrostatic forces for high contact resistances) are more easily overcome by elastic recovering forces. The devices present an I_{ON}/I_{OFF} ratio bigger than 10^3, limited by the instrument compliance current.

However, it was found that the reliability of the fabricated devices was low, working just for one or two cycles. In order to solve this problem an atomic layer deposition (ALD) was performed depositing 8nm of Al_2O_3 oxide [16]. Figure 3 B) shows its electrical response. It can be appreciated how the snap-in event takes place at lower voltage value (5 V) due to the reduction of the gap and the accumulation of charges in the dielectric layer [17]. An improved I_{ON}/I_{OFF} ratio (10^4) is obtained and an abrupt behavior of at least 5 mV/decade, beating CMOS limit. Moreover, the device works for ten cycles, improving its reliability.

3. Conclusions

Successful fabrication of NEMS switches in a commercial CMOS technology has been demonstrated, obtaining CMOS operating voltages (5V) due to the small gap defined (27 nm). Comparing with the features of the state of the art devices (table 1), it can be appreciated how the developed device present similar characteristics in terms of I_{ON}/I_{OFF} ratio and abrupt behavior. In addition it present the advantage of an easy fabrication process, reduced dimensions that make it suitable for high integration density and the robust and reproducible fabrication process that CMOS technologies offer.

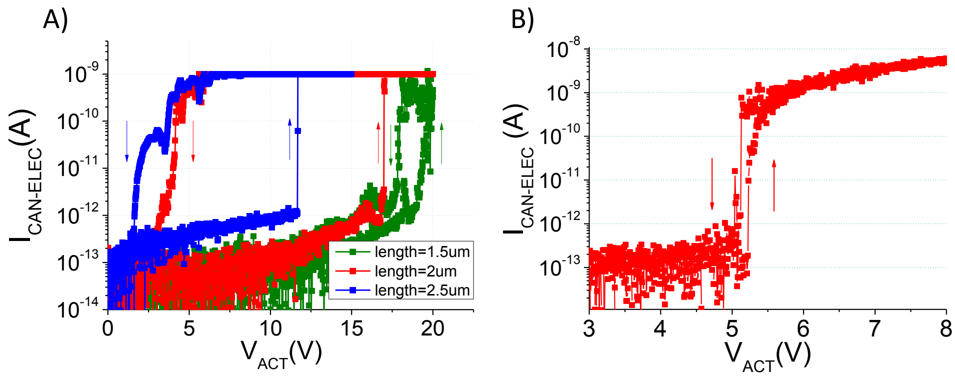

Fig. 2) (A) Electrical measurement for different cantilever length. (B) Cantilever switch (1.5 µm length) electrical characterization after ALD process (8nm AL_2O_3 oxide).

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